

2.5V 16-Bit Bus Transceiver and Register with 3-State Outputs

Product Features

- PI74AVC+16646 is designed for low voltage operation, $V_{CC} = 1.65V$ to $3.6V$
- True $\pm 24mA$ Balanced Drive @ $3.3V$
- I_{OFF} supports partial power-down operation
- $3.6V$ I/O Tolerant Inputs and Outputs
- All outputs contain a patented DDC (Dynamic DriveControl) circuit that reduces noise without degrading propagation delay.
- Industrial operation at $-40^{\circ}C$ to $+85^{\circ}C$
- Available Packages:
 - 56-pin 240 mil wide plastic TSSOP (A)
 - 56-pin 173 mil wide plastic TVSOP (K)

Product Description

Pericom Semiconductor’s PI74AVC+ series of logic circuits are produced using the Company’s advanced sub-micron CMOS technology, achieving industry leading speed.

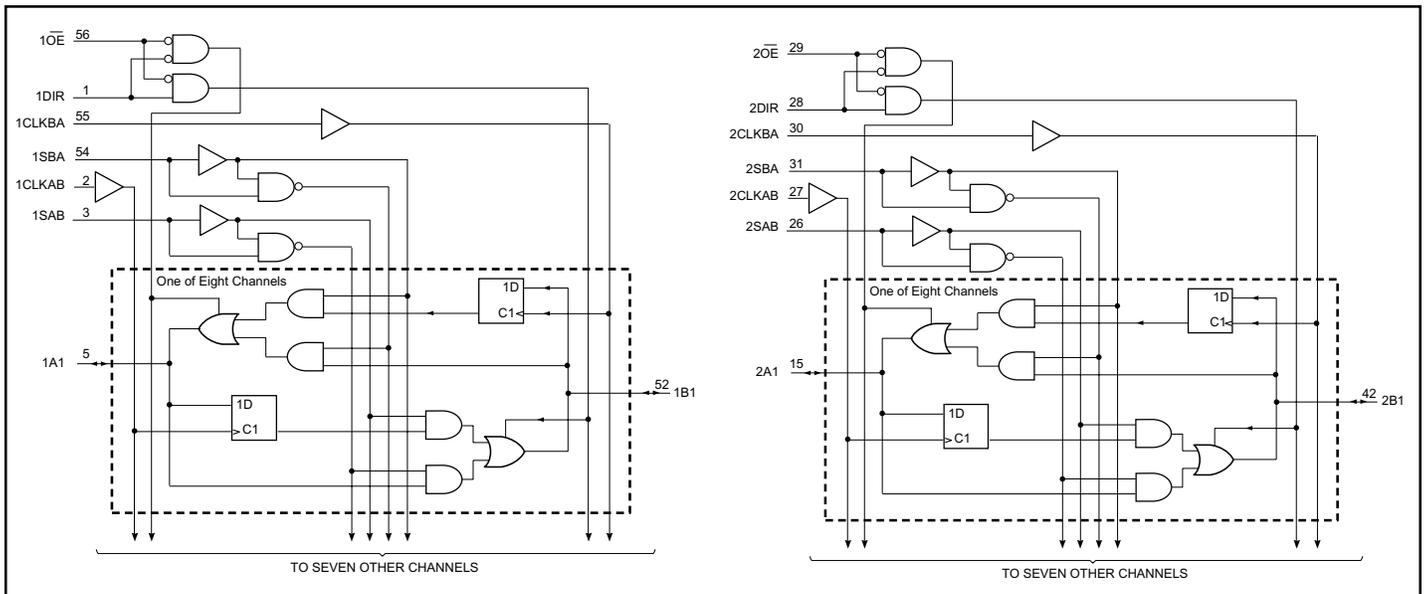
The PI74AVC+16646 is a 16-bit bus transceiver and register designed for $1.65V$ to $3.6V$ V_{CC} operation. It can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate Clock (CLKAB or CLKBA) input. Four fundamental bus-management functions can be performed.

Output Enable (\overline{OE}) and Direction Control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The Select Control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. Circuitry used for Select Control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. DIR determines which bus receives data when \overline{OE} is LOW. In the isolation mode (\overline{OE} HIGH), A data may be stored in one register and/or B data may be stored in the other register.

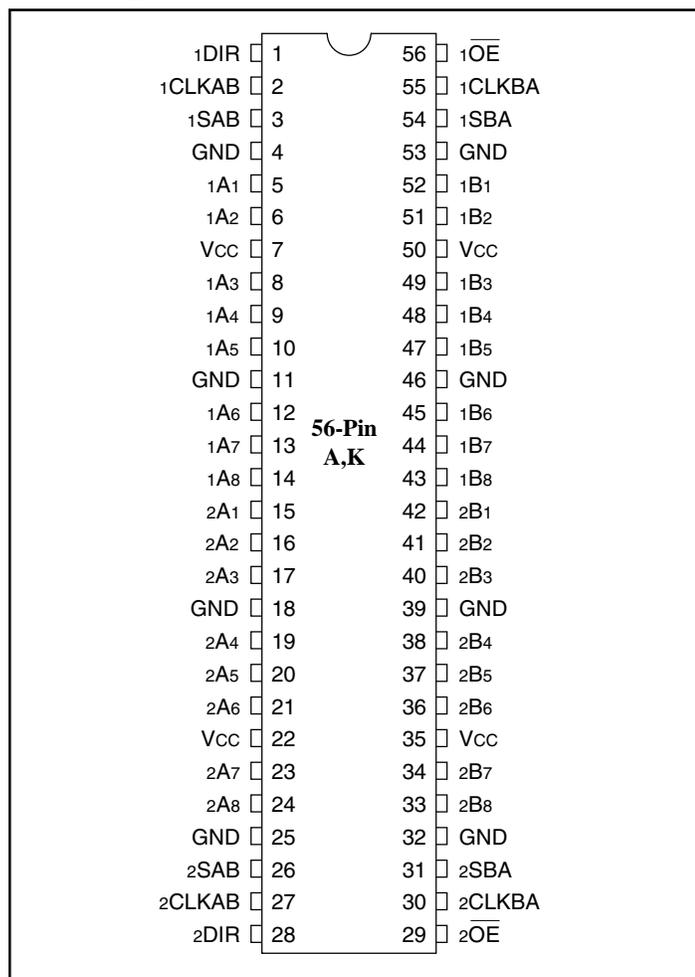
When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Logic Block Diagrams



Pin Configuration



Product Pin Description

Pin Name	Description
xOE	Output Enable Inputs (Active LOW)
xDIR	Direction Control
xCLKAB, xCLKBA	Clock Pulse Inputs
xSAB, xSBA	Select Control Inputs
xAx	Data Register A Inputs Data Register B Outputs
xBx	Data Register B Inputs Data Register A Outputs
GND	Ground
VCC	Power

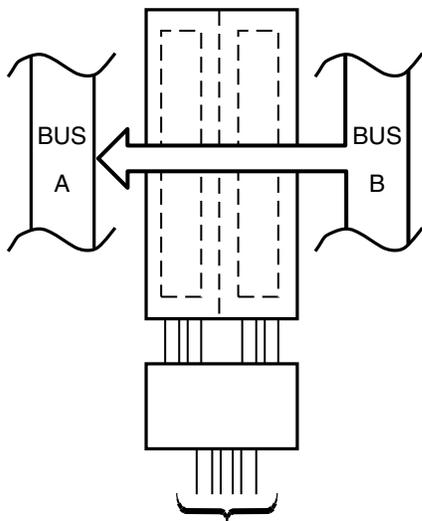
Truth Table

Function	Inputs						Data I/O	
	xOE	xDIR	xCLKAB	xCLKBA	xSAB	xSBA	xAx	xBx
Store A, B Unspecified ⁽¹⁾ Store B, A Unspecified ⁽¹⁾	X	X	↑	X	X	X	Input Unspecified ⁽¹⁾	Unspecified ⁽¹⁾ Input
Isolation, Hold Storage Store A and B Data	H	X	H or L ↑	H or L ↑	X	X	Input Disable Input	Input Disable Input
Real Time A Data to B Bus Stored A Data to B Bus	L	H	X H or L	X X	L H	X X	Input Input	Output Output
Real Time B Data to A Bus Stored B Data to A Bus	L	L	X X	X H or L	X X	L H	Output Output	Input Input

Notes:

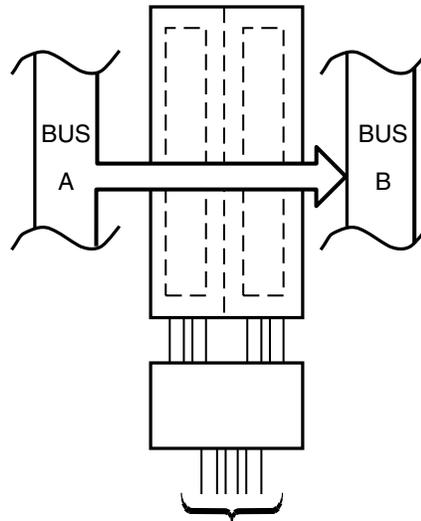
1. The data output functions may be enabled or disabled by various signals at the xOE or xDIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
2. H= High Voltage Level
X = Don't Care
L= Low Voltage Level
↑ = LOW-to-HIGH transition

REAL-TIME TRANSFER
BUS B to A



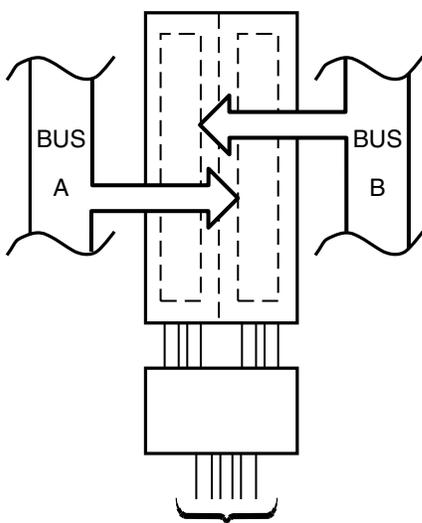
xDIR	$\overline{\text{xOE}}$	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS A to B



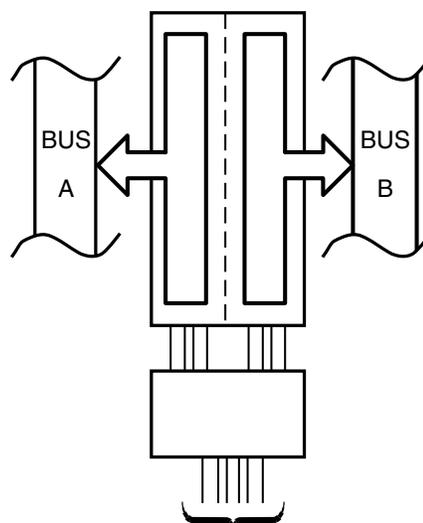
xDIR	$\overline{\text{xOE}}$	xCLKAB	xCLKBA	xSAB	xSBA
H	L	X	X	L	X

STORAGE FROM
A,B, or A and B



xDIR	$\overline{\text{xOE}}$	xCLKAB	xCLKBA	xSAB	xSBA
X	X	↑	X	X	X
X	X	X	↑	X	X
X	H	↑	↑	X	X

TRANSFER STORED
DATA to A and/or B



xDIR	$\overline{\text{xOE}}$	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	HorL	X	H
H	L	HorL	X	H	X

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply voltage range, V_{CC}	-0.5V to +4.6V
Input voltage range, V_I	-0.5V to +4.6V
Voltage range applied to any output in the high-impedance or power-off state, $V_O^{(1)}$	-0.5V to +4.6V
Voltage range applied to any output in the high or low state, $V_O^{(1,2)}$	-0.5V to $V_{CC} + 0.5V$
Input clamp current, I_{IK} ($V_I < 0$)	-50mA
Output clamp current, I_{OK} ($V_O < 0$)	-50mA
Continuous output current, I_O	$\pm 50mA$
Continuous current through each V_{CC} or GND	$\pm 100mA$
Package thermal impedance, $\theta_{JA}^{(3)}$: package A	64°C/W
package K	48°C/W
Storage Temperature range, T_{stg}	-65°C to 150°C

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Notes:

1. Input & output negative-voltage ratings may be exceeded if the input and output current rating are observed.
2. Output positive-voltage rating may be exceeded up to 4.6V maximum if the output current rating is observed.
3. The package thermal impedance is calculated in accordance with JESD 51.

Recommended Operating Conditions⁽¹⁾

		Min.	Max.	Units
V_{CC} Supply Voltage	Operating	1.65	3.6	V
	Data retention only	1.2		
V_{IH} High-level Input Voltage	$V_{CC} = 1.2V$	V_{CC}		
	$V_{CC} = 1.65V$ to 1.95V	$0.65 \times V_{CC}$		
	$V_{CC} = 2.3V$ to 2.7V	1.7		
	$V_{CC} = 3V$ to 3.6V	2		
V_{IL} Low-level Input Voltage	$V_{CC} = 1.2V$		Gnd	
	$V_{CC} = 1.65V$ to 1.95V		$0.35 \times V_{CC}$	
	$V_{CC} = 2.3V$ to 2.7V		0.7	
	$V_{CC} = 3V$ to 3.6V		0.8	
V_I Input Voltage		0	3.6	
V_O Output Voltage	Active State	0	V_{CC}	
	3-State	0	3.6	
I_{OH} High-level output current	$V_{CC} = 1.65V$ to 1.95V		-6	mA
	$V_{CC} = 2.3V$ to 2.7V		-12	
	$V_{CC} = 3V$ to 3.6V		-24	
I_{OL} Low-level output current	$V_{CC} = 1.65V$ to 1.95V		6	
	$V_{CC} = 2.3V$ to 2.7V		12	
	$V_{CC} = 3V$ to 3.6V		24	
$\Delta t_{\Delta v}$ Input transition rise or fall rate	$V_{CC} = 1.65V$ to 3.6V		5	ns/V
T_A Operating free-air temperature		-40	85	°C

Notes:

1. All unused inputs must be held at V_{CC} or GND to ensure proper device operation.

DC Electrical Characteristics (Over the Operating Range, $T_A = -40^{\circ}\text{C} + 85^{\circ}\text{C}$)

Parameters		Test Conditions ⁽¹⁾	V _{CC}	Min.	Max.	Units
V _{OH}		I _{OH} = -100μA	1.65V to 3.6V	V _{CC} - 0.2V		V
		I _{OH} = -6mA V _{IH} = 1.07V	1.65V	1.2		
		I _{OH} = -12mA V _{IH} = 1.7V	2.3V	1.75		
		I _{OH} = -24mA V _{IH} = 2V	3V	2.0		
V _{OL}		I _{OL} = 100μA	1.65V to 3.6V		0.2	V
		I _{OL} = 6mA V _{IH} = 0.57V	1.65V		0.45	
		I _{OL} = 12mA V _{IH} = 0.7V	2.3V		0.55	
		I _{OL} = 24mA V _{IH} = 0.8V	3V		0.8	
I _I	Control Inputs	V _I = V _{CC} or GND	3.6V		±2.5	μA
	I _{OFF}	V _I or V _O = 3.6V	0		±10	
	I _{OZ}	V _I = V _{CC} or GND	3.6V		±10	
	I _{CC}	V _O = V _{CC} or GND I _O = 0	3.6V		40	
C _I	Control Inputs	V _I = V _{CC} or GND	2.5V		4	pF
			3.3V		4	
	Data Inputs		2.5V		6	
			3.3V		6	
C _O	Outputs	V _O = V _{CC} or GND	2.5V		8	
			3.3V		8	

Note: Typical values are measured at T_A = 25°C.

Timing Requirements

(Over recommended operating free-air temperature range, unless otherwise noted, see Figures 1 thru 4)

	V _{CC} = 1.2V		V _{CC} = 1.5V ±0.1V		V _{CC} = 1.8V ±0.15V		V _{CC} = 2.5V ±0.2V		V _{CC} = 3.3V ±0.3V		Units
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
f _{clock} Clock Frequency						150		250		350	MHz
t _w Pulse duration, CLKAB or CLKBA high or low					3.0		2.0		1.4		ns
t _{su} Setup time, A before CLKAB↑, or B before CLKBA↑					1.9		0.9		0.8		
t _h Hold time, A after CLKAB↑, or B after CLKBA↑					0.8		0.5		0.6		

Switching Characteristics

(Over recommended operating free-air temperature range, unless otherwise noted, see Figures 1 thru 4)

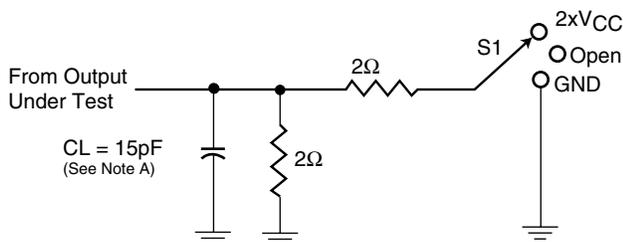
Parameters	From (Input)	To (Output)	V _{CC} = 1.2V		V _{CC} = 1.5V ±0.1V		V _{CC} = 1.8V ±0.15V		V _{CC} = 2.5V ±0.2V		V _{CC} = 3.3V ±0.3V		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f _{max}							150		250		350		MHz
t _{pd}	A or B	B or A					1.5	3.5	1.2	2.5	0.9	2.0	ns
	CLKAB or CLKBA	A or B					1.9	4.2	1.3	2.8	1.0	2.5	
	SAB or SBA						1.9	3.8	1.8	3.0	1.5	2.5	
t _{en}	OE						1.9	4.5	1.4	3.5	1.0	3.0	
t _{dis}						1.9	4.0	1.4	3.5	1.0	3.0		
t _{en}	DIR					1.9	4.5	1.4	3.5	1.0	3.0		
t _{dis}						1.9	4.0	1.4	3.0	1.0	3.0		

Operating Characteristics T_A = 25°C

Parameters		Test Conditions	V _{CC} = 1.8V ±0.15V	V _{CC} = 2.5V ±0.2V	V _{CC} = 3.3V ±0.3V	Units
			Typical	Typical	Typical	
Cpd Power Dissipation Capacitance	Outputs Enabled	C _L = 0pF, f = 10 MHz	23	25	30	pF
	Outputs Disabled		5	6	10	

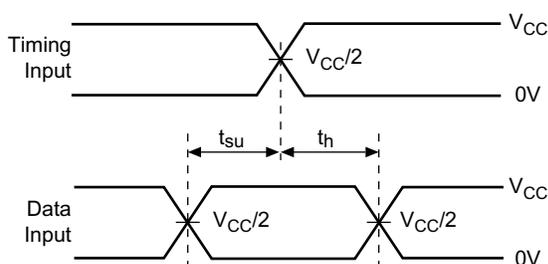
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 1.2V$ AND $1.5V \pm 0.1V$

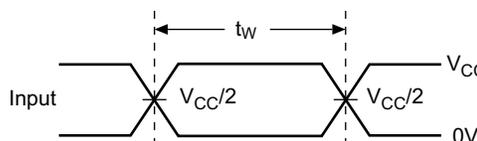


Load Circuit

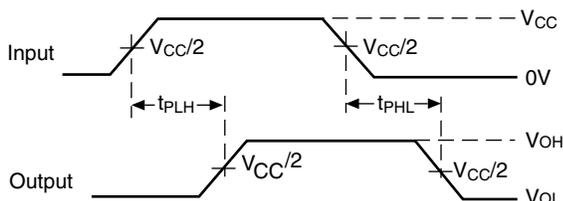
Test	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open $2 \times V_{CC}$ GND



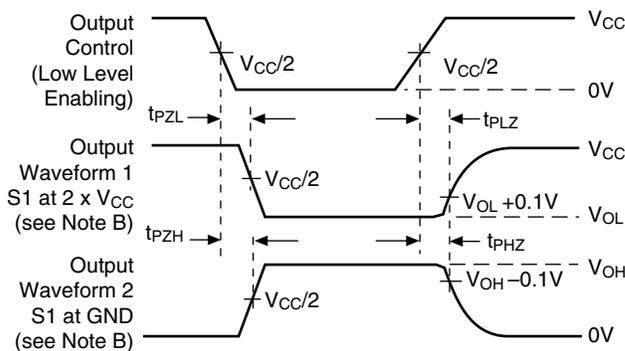
Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Pulse Duration



Voltage Waveforms
Propagation Delay Times



Voltage Waveforms
Enable and Disable Times

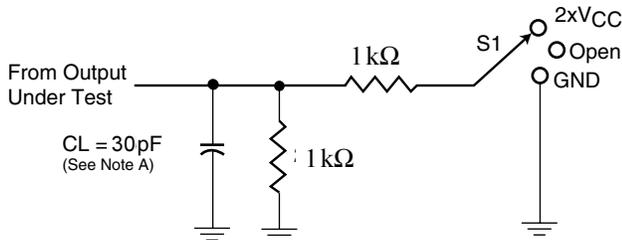
Figure 1. Load Circuit and Voltage Waveforms

Notes:

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input impulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50\Omega$, $t_R \leq 2.0$ ns, $t_F \leq 2.0$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}
- F. t_{PZL} and t_{PZH} are the same as t_{en}
- G. t_{PLH} and t_{PHL} are the same as t_{pd}

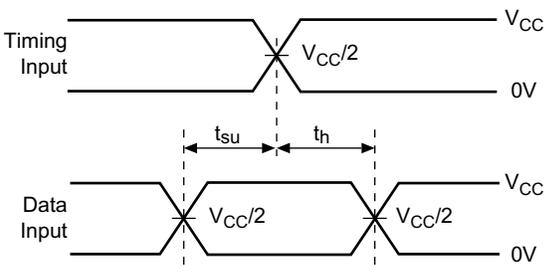
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 1.8V \pm 0.15V$

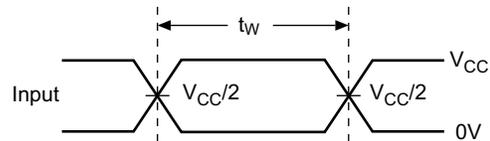


Load Circuit

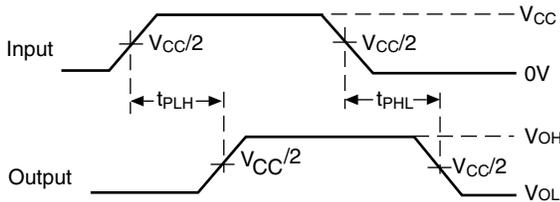
Test	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open $2 \times V_{CC}$ GND



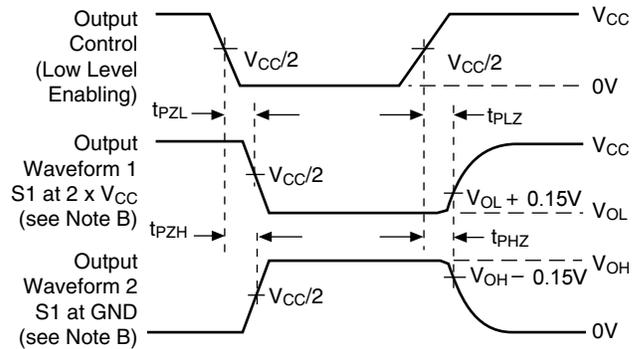
Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Pulse Duration



Voltage Waveforms
Propagation Delay Times



Voltage Waveforms
Enable and Disable Times

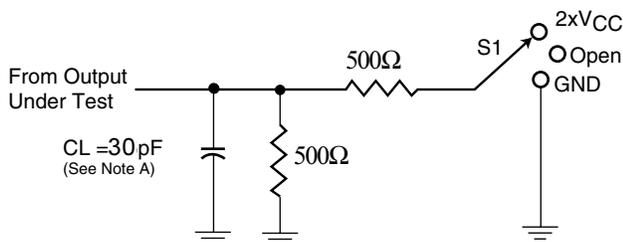
Figure 2. Load Circuit and Voltage Waveforms

Notes:

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input impulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50\Omega$, $t_R \leq 2.0ns$, $t_F \leq 2.0ns$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}
- F. t_{PZL} and t_{PZH} are the same as t_{en}
- G. t_{PLH} and t_{PHL} are the same as t_{pd}

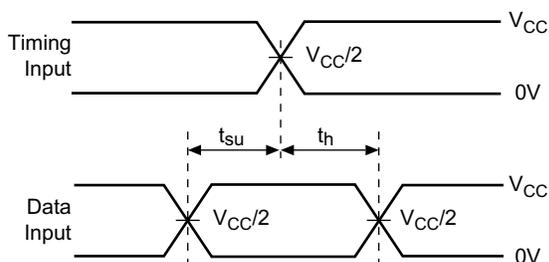
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.5V \pm 0.2V$

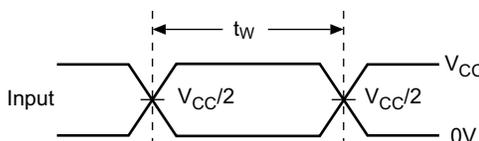


Load Circuit

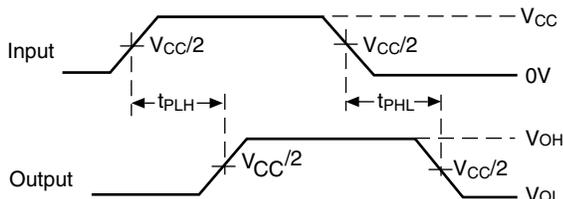
Test	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open $2 \times V_{CC}$ GND



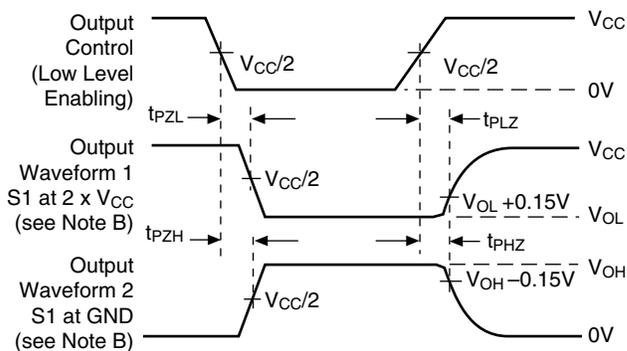
Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Pulse Duration



Voltage Waveforms
Propagation Delay Times



Voltage Waveforms
Enable and Disable Times

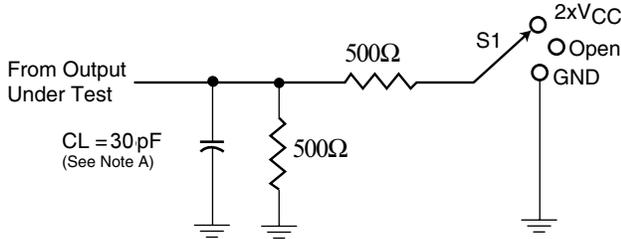
Figure 3. Load Circuit and Voltage Waveforms

Notes:

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input impulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50\Omega$, $t_R \leq 2.0\text{ns}$, $t_F \leq 2.0\text{ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}
- F. t_{PZL} and t_{PZH} are the same as t_{en}
- G. t_{PLH} and t_{PHL} are the same as t_{pd}

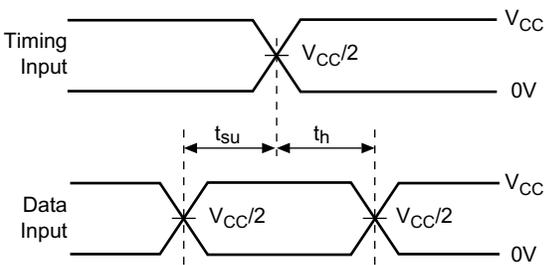
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 3.3V \pm 0.3V$

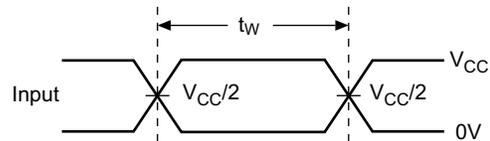


Load Circuit

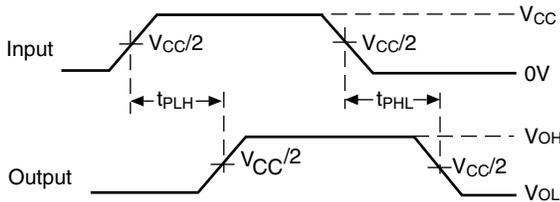
Test	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open $2 \times V_{CC}$ GND



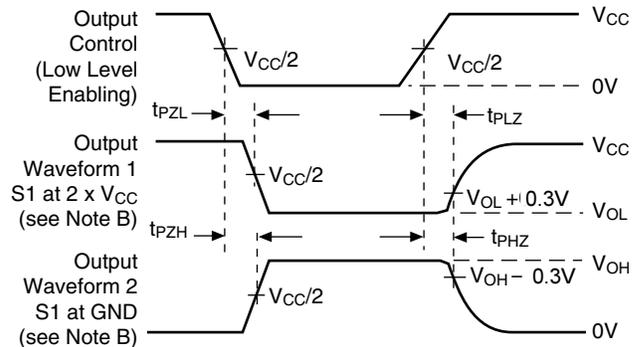
Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Pulse Duration



Voltage Waveforms
Propagation Delay Times



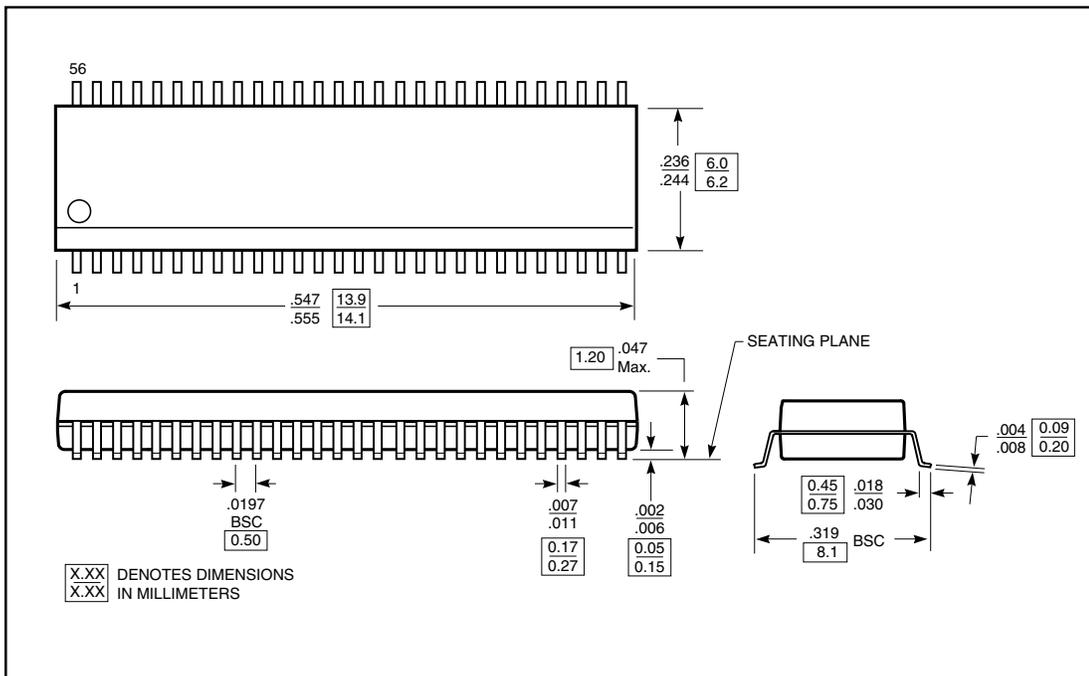
Voltage Waveforms
Enable and Disable Times

Figure 4. Load Circuit and Voltage Waveforms

Notes:

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input impulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50\Omega$, $t_R \leq 2.0\text{ns}$, $t_F \leq 2.0\text{ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}
- F. t_{PZL} and t_{PZH} are the same as t_{en}
- G. t_{PLH} and t_{PHL} are the same as t_{pd}

56-Pin TSSOP



56-Pin TVSOP

